Remarks

Applicants respectfully request reconsideration of this application as amended. Claims 1-3 and 5-26 have been amended. No claims have been cancelled. Therefore, claims 1-26 are presented for examination.

Claims 1-26 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of the standard practice of integrating circuits, as further evidenced by Sherburne (U.S. Pub. No. 2002/0184546). Applicants submit that the present claims are patentable over the combination of Arimilli and Sherburne.

Arimilli discloses a system for managing a data access transaction within a hierarchical data storage system. See Arimilli at Abstract. The system includes a symmetric multiprocessor (SMP) system including a plurality of processors. Each processor includes a respective level one (L1) cache. Each processor is coupled via a processor bus to a level two cache, which are in-line caches shared by multiple processors. Each L2 cache is connected to a level three (L3) cache and to a system bus. The lower cache levels are employed to stage data to the L1 caches. L2 caches and L3 caches thus serve as intermediate storage between the processors and system memory. The L2 caches and L3 caches are connected to system memory via the system bus col. 4, ll. 8-64. Nonetheless, Arimilli does not disclose or suggest control logic to receive a first cache line from a first dedicated processor cache and to transfer the first cache line to a second dedicated processor cache.

Sherburne discloses a low power configurable processor core. See Sherburne at Abstract. However, Sherburne does not disclose or suggest control logic to receive a first cache line from a first dedicated processor cache and to transfer the first cache line to a second dedicated processor cache.

Claim 1 of the present application recites control logic coupled to first and second dedicated caches to receive a first cache line from the first dedicated cache and to transfer the first cache line to the second dedicated cache. As discussed above, neither Arimilli nor Sherburne disclose or suggest transferring a cache line from a first dedicated processor cache and to transfer the first cache line to a second dedicated processor cache. Arimilli discloses an architecture having dedicated processor caches. However, there is no disclosure of control logic that transfers cache lines between the dedicated processor caches.

Since neither Arimilli nor Sherburne disclose or suggest transferring a cache line from a first dedicated processor cache and to transfer the first cache line to a second dedicated processor cache, any combination of Arimilli and Sherburne would not disclose or suggest such a feature. Thus, claim 1 is patentable over Arimilli in view of Sherburne. Claims 2-11 depend from claim 1 and include additional features. Therefore, claims 2-11 are also patentable over Arimilli in view of Sherburne.

Claim 12 recites transferring a first cache line from a first dedicated cache of a chip multi-processor to control logic in the chip multi-processor and subsequently transferring the first cache line from the control logic to a second dedicated cache of the chip multi-processor. For the reasons described above with respect to clam 1, claim 12 is also patentable over Arimilli in view of Sherburne. Because claims 13-17 depend from claim 12 and include additional features, claims 13-17 are also patentable over Arimilli in view of Sherburne.

Claim 18 control logic coupled to first and second dedicated caches to receive a first cache line from the first dedicated cache and to transfer the first cache line to the second dedicated cache. Thus, for the reasons described above with respect to clam 1, claim 18 is

also patentable over Arimilli in view of Sherburne. Since claims 19-22 depend from claim 12 and include additional features, claims 13-17 are also patentable over Arimilli in view of Sherburne.

Claim 22 recites transferring a first cache line from a first dedicated cache of a chip multi-processor to control logic in the chip multi-processor and subsequently transferring the first cache line from the control logic to a second dedicated cache of the chip multi-processor. For the reasons described above with respect to clam 1, claim 22 is also patentable over Arimilli in view of Sherburne. Because claims 23-26 depend from claim 12 and include additional features, claims 23-26 are also patentable over Arimilli in view of Sherburne.

Applicants respectfully submit that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Applicants respectfully petition for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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